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In re Application of:	)	
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Etsuyoshi KOBORI	)	
	)	Group Art Unit: 2814
Application No. 09/610,148	)	
	)	Examiner: Anh D. Mai
Filed: July 5, 2000	)	
	)	**Mail Stop AF**
For: METHOD OF FABRICATING SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE	)	

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Sir:

VERIFICATION OF A TRANSLATION

I, the below named translator, hereby declare that:

My name and post office address are as stated below;

That I am knowledgeable in the English language and in the Japanese language and believe the attached English translation to be a true and complete translation of the below identified document.

The document for which the attached English translation is being submitted is the Japanese Patent Application No. 10-037178, filed in Japan on February 19, 1998.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature of the translator: 

Date: July 17, 2003.

[Document Name] Specification

[Title of Invention] METHOD OF WIRING SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE IN WHICH WIRING IS FORMED

[Scope of Claims]

[Claim 1]

A method of wiring a semiconductor device, comprising the steps of:

forming a first-wiring use groove and a second-wiring use groove apart therefrom, each being formed on a first insulation layer;

forming a conductive layer by embedding conductive material into a first and a second wiring grooves and form the conductive layer to cover the first insulating layer;

performing an ion implantation by implanting oxygen from an upper space of the conductive layer to oxidize a part of the conductive layer to form an insulation between the first wiring groove and the second wiring groove to be electrically insulated from each other.

[Claim 2]

A method of wiring a semiconductor device according to claim 1, the ion implantation by oxygen is performed in a way such that a part of the conductive layer being located at higher position from the first insulation layer is oxidized.

[Claim 3]

A method of wiring a semiconductor device according to claim 2, the ion implantation by oxygen is performed in a way such that upper portions of the first wiring and the second wiring are oxidized.

[Claim 4]

A method of wiring a semiconductor device according to any one of the claims 1-3, the passivation layer is further formed on the oxidized conductive layer.

[Claim 5]

A semiconductor device comprising:

a first wiring of which wiring is embedded in a first insulation layer;

a second wiring of which wiring is embedded in a first insulation layer to be formed apart from the first wiring;

a non-conductive layer which is constituted by oxidizing a metal material of the first and the second wirings, said non-conductive layer abutting to the first and the second wirings, and covering the fist insulation layer.

[Detailed Description of the Invention]

[Technical Field of the Invention]

The present invention relates to a method of fabricating a semiconductor device. More particularly, the present invention relates to a simplification of a process of fabricating a semiconductor device.

[Conventional Art and Problems to be Solved]

Recently, a method of wiring of Dual-Damascene structure comes to be known, in which upper metal wires 8a and 8b are embedded in an insulating layer as shown in Fig. 3. When the Dual-Damascene structure is adopted, it becomes possible to form wiring made of a material such as copper, which is difficult to be etched.

Referring to Fig. 4, a method of fabricating a wiring of the Dual-Damascene structure will be explained below. First, a resist pattern used for forming contact holes is formed on the SiO_2 layer 2, and the SiO_2 layer 2 is selectively etched to form contact holes. Successively, a resist pattern used for forming grooves is formed and etched to form grooves. Due to the foregoing, as shown in Fig. 4A, a groove 6a for the first wiring section, contact hole 4a, groove 6b for the second wiring section and contact hole 4b are formed. Fig. 4B is a view taken in the direction of arrow A in Fig. 4A.

Then, copper 11 is deposited all over the surface by the method of plating. Due to the foregoing, the copper film is embedded in the grooves 6 as well as in the contact holes 4, and an upper surface of the SiO_2 layer 2 is covered with the copper 11 as shown in Fig. 4C.

Next, copper, except for the portions of the grooves 6 and the contact holes 4, is removed by the method of

chemical mechanical polishing (CMP method). Due to the foregoing, the first wiring section 18 and the second wiring section 19 are insulated from each other as shown in Fig. 3.

However, according to the above fabrication method, the following problems may be encountered in case of absent of the CPM method such that insulation between the first wiring section 18 and the second wiring section 19 can not be made. In this sense, the CMP apparatus is additionally required for the above fabrication method. Moreover, when the CMP method is adopted, it is necessary to select appropriate chemicals and abrasive materials. Accordingly, when a wiring layer is made of a new metal, much more time and expense are required for their investigation.

It is an object of the present invention to solve the above problems and provide a method of wiring a semiconductor device by which a plurality of wiring patterns can be isolated from one another without using the CMP method.

[Problems that the Invention is to Solve]

According to a method of wiring a semiconductor device, it comprises the steps of: embedding conductive material into a first and a second wiring grooves ; performing an ion implantation which implants oxygen onto the conductive layer being formed over the first insulating

layer; and oxidizing a part of the conductive layer to form an insulation between the first wiring groove and the second wiring groove to be electrically insulated from each other. Therefore, insulation between the first wiring and the second wiring is securely made without removing the conductive layer.

According to a method of wiring a semiconductor device, the oxygen ion implantation, the oxygen ion implantation is performed in the way such that upper portions of the first and the second wirings are oxidized so as to secure the oxidation of the conductive layer being located at higher position from the first insulation layer. Therefore, the first wiring and the second wiring are securely insulated from each other.

According to a method of wiring a semiconductor device, an insulation layer is further formed on the oxidized semiconductor layer, by which the first wiring and the second wiring is securely insulated from each other.

According to a method of wiring a semiconductor device, the non-conductive layer is constituted by oxidizing the metal material of the first and the second wirings and it abuts to the first and the second wirings, and simultaneously covers the fist insulation layer. Therefore, insulation between the first wiring and the

second wiring is securely made without removing the conductive layer.

[Mode for Carrying Out the Invention]

Referring to the accompanying drawings, a method of wiring in the present invention will be explained below.

First, in the same manner as that of the conventional method of fabricating, copper is deposited as illustrated in Fig. 3C. Starting from this condition, ion implantation is performed by implanting oxygen ion under such a condition that oxygen reaches the depth from the upper surface to the position which is deeper than the thickness t1 of the copper 11 formed on the SiO_2 layer 2 as shown in Fig. 1A.

Due to the foregoing, the copper formed on the SiO_2 layer 2 and the copper at the upper portions of the first wiring section 18 and the second wiring section 19 are oxidized, and as a result an oxidation layer 13 is formed as shown in Fig. 1C. Since the dielectric constant of copper oxide is high, the first wiring section 18 and the second wiring section 19 are properly insulated from each other. Furthermore, it is possible to form an passivation film 15 on the oxidation layer 13 which secures the insulation in case of forming another wiring on the upper surface.

As described above, the wiring of the Dual-Damascene structure can be formed. As shown in Fig. 2, the first wiring section 18 and the second wiring section 19 are formed in the SiO_2 layer 2. The first wiring section 18 is provided with a plug 9a and a first metal wire 8a. In the same manner, the second wiring section 19 is provided with a plug 9b and a second metal wire 8b. An oxidation layer 13 made of copper oxide is formed on the SiO_2 layer 2. In this connection, concerning the upper layers of the first metal wire 8a and the second metal wire 8b, oxidation is conducted to a position which is slightly deeper than the upper surface of the SiO_2 layer 2. Further, the passivation layer 15 is further formed on the oxidation layer 13.

As described above, unlike the conventional method such that the copper 11 except for the first metal wire 8a and the second metal wire 8b is removed, the copper is oxidized so as to be changed into an insulator, which eliminates the need of a copper film removing process by the method of CMP being used.

In this embodiment, wiring is made of copper. However, the present invention is not limited to the above specific embodiment. As long as a conductive layer is used as wiring, the present invention can be applied to any conductive layer. Examples of material of the conductive

layer is aluminum. Also, the present invention can be applied to metal of which principle component is aluminum or copper, such as aluminum silicon (AlSi) or aluminum silicon copper (AlSiCu). Furthermore, the present invention can be applied to a chemical compound of aluminum and tungsten or a chemical compound of copper and tungsten. Concerning aluminum, abrasive and solvent used for removing aluminum by the CMP method have not been developed at present. Accordingly, when the wiring method of the present invention is used, aluminum can be used for the wiring of the Dual-Damascene structure.

In this embodiment, oxygen ions are implanted to a position slightly deeper than the upper surface of the SiO_2 layer 2. However, if it is possible to perform highly accurate control of the depth of implantation of ions to the level where positively insulation can be made between the first wiring section 18 and the second wiring section 19 from each other, oxygen ions may be implanted to the same depth as that of the upper surface of the SiO_2 layer 2.

In this embodiment, the present invention is applied to a case in which the shallow grooves for wiring of the Dual-Damascene structure are formed and also the deep holes are formed. However, the present invention is not limited to the Dual-Damascene structure. In the case where a

groove is formed on an insulating layer and a conductor is embedded in the groove, the present invention can be also applied.

[BRIEF DESCRIPTION OF THE DRAWINGS]

Fig. 1 is the views showing a process of fabricating a wiring in the present invention;

Fig. 2 is a cross-sectional view showing main part of a wiring structure in the present invention;

Fig. 3 is a cross-sectional view showing a primary portion of a semiconductor device for explaining the Dual-Damascene structure; and

Fig. 4 is the views showing a conventional fabricating processes.

[DESCRIPTION OF THE REFERENCE NUMERALS]

2 SiO2 layer

13 Oxidized layer

18 First wiring section

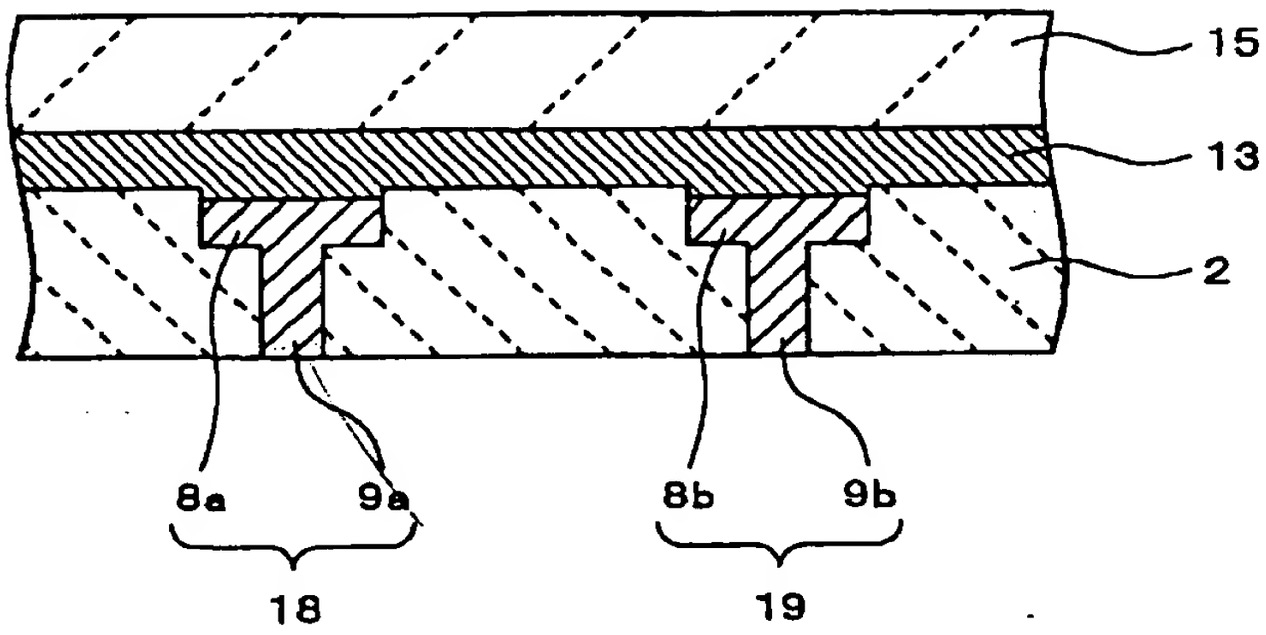
19 Second wiring section

ABSTRACT

Wiring of the Dual-Damascene structure is formed without using the CMP method.

As shown in Fig. 1A, oxygen ions are implanted from an upper surface under the condition that the oxygen ions reach a position a little deeper than the thickness t1 of the copper film 11 on the SiO_2 layer 2. Due to the foregoing, as shown in Fig. 1B, the copper film 11 on the SiO_2 layer 2 and the copper films on the upper portions of the first wiring section 18 and the second wiring section 19 are oxidized, and the oxidized layer 13 is formed. Since the dielectric constant of copper oxide is high, the first wiring section 18 and the second wiring section 19 are insulated from each other. Therefore, it is possible to obtain a highly reliable wiring structure easily.

Fig. 2



13:酸化層
Oxidation layer

Fig. 3

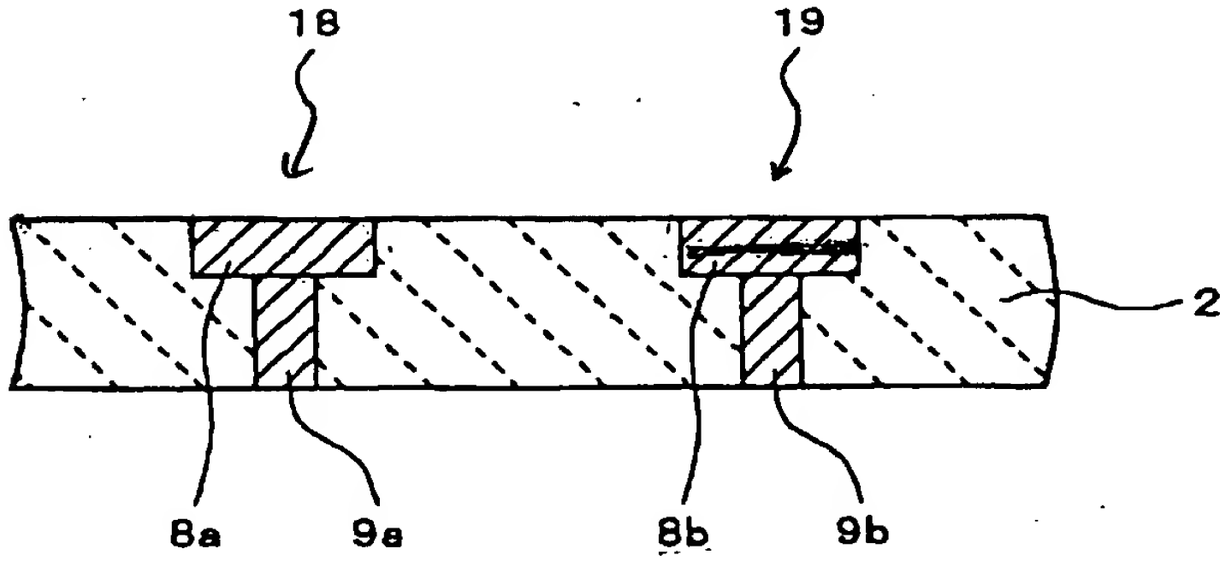
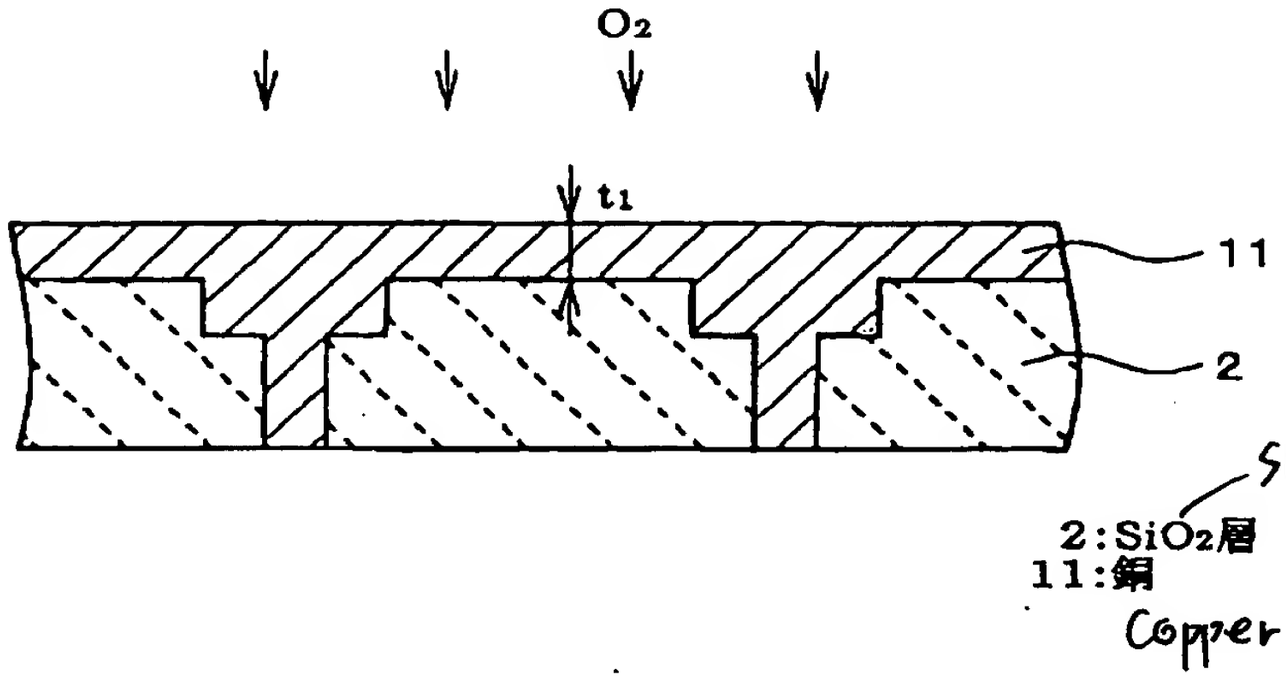


Fig. 1

A



B

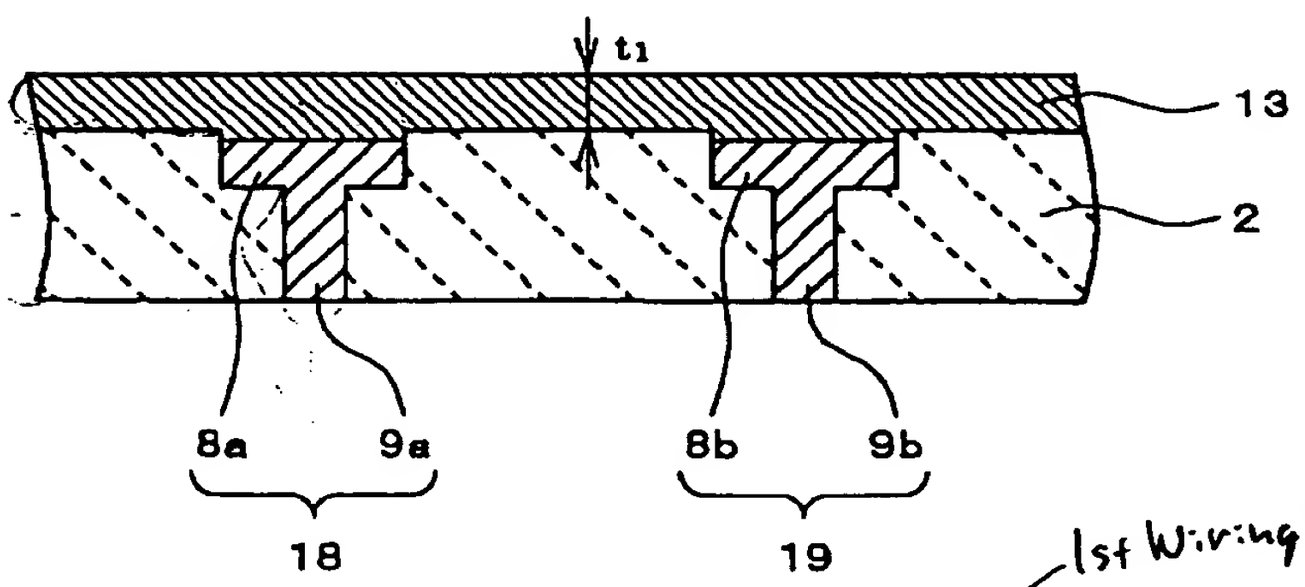
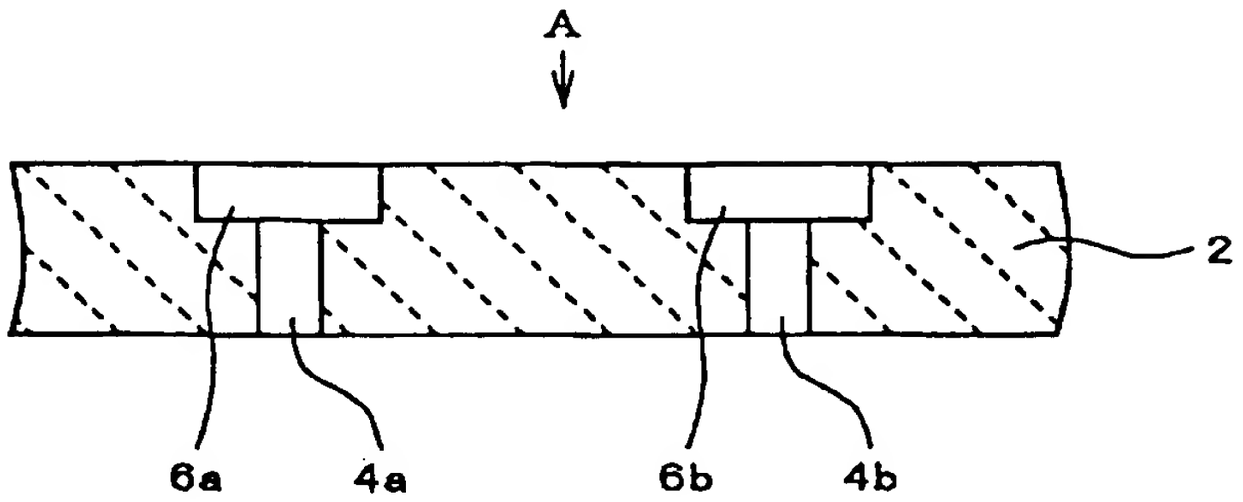


Fig.4

A



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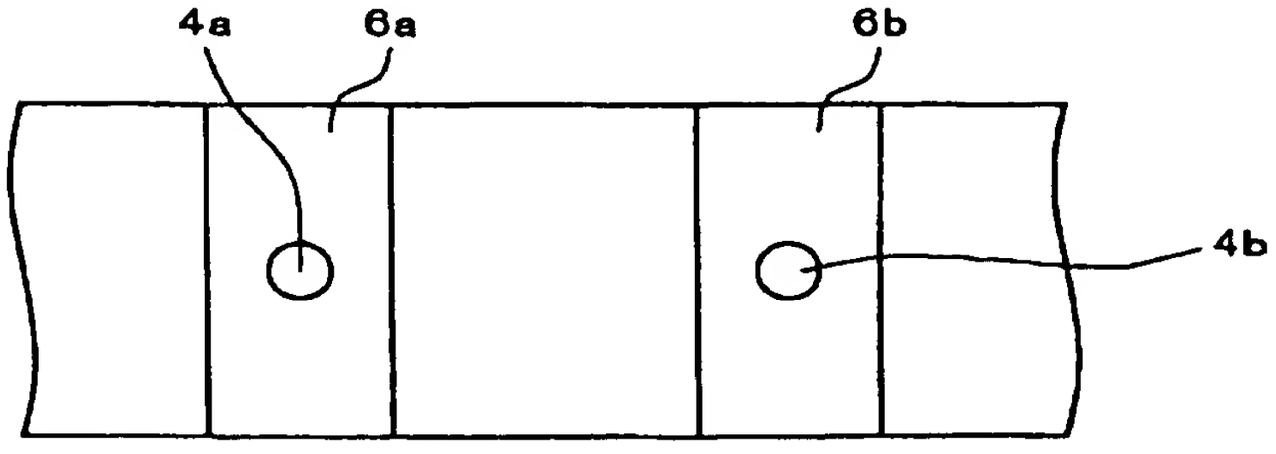

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